

**REMARKS/ARGUMENTS**

**Objection of claims 8-9 under 37 CFR 1.75 as being a substantial duplicate of claim 1.**

5       Claims 8-9 are canceled and are no longer in need of consideration.

**Rejection of claims 1, 3-6 and 8-19 under 35 U.S.C 103(a) as being unpatentable over Applicant's admitted prior art (APA), figures 1-2, in view of Sato, US**

10      **2006/0097380.**

15       Claim 1 of the present invention recites a liquid crystal display module having a glass substrate, at least a gate driver chip mounted directed on the peripheral area of the glass substrate, and at least a source driver chip mounted directly on the peripheral area of the glass substrate. The thickness of the gate driver chip and the source driver chip is preferably less than 0.3 mm.

20       Claim 13 recites a liquid crystal display module having a glass substrate and at least a driver chip mounted directly on the peripheral area of the glass substrate, in which the thickness of the driver chip is less than 0.3 mm.

25       Despite Sato discloses a driver chip having a thickness of less than 0.3 mm, applicant asserts that this driver chip is not mounted directly on a glass substrate, as stated in claims 1 and 13 of the present invention. Instead, the driver IC chip 9 disclosed by Sato is placed on a circuit board composed of a resin plate 25 and a plurality of wiring lines 29, as indicated in Fig. 2 and paragraph [0027] to [0031] of the cited reference.

30       Moreover, the present invention specifically discloses that the gate/source driver chip are fabricated to effectively improve the curtain mura phenomenon commonly

found in conventional liquid crystal display modules. Despite Sato in paragraph [0067] teaches the thickness of the driver IC chip can be 0.140 mm, Sato never suggested the driver IC chip could be applied to a liquid crystal display module and the reduced thickness of the driver IC chip could be used to improve the curtain mura 5 phenomenon commonly found in a liquid crystal display module.

According to MPEP 2141.01(a), in order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the filed of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem 10 with which the inventor was concerned. *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 4776, 1445 (Fed. Cir. 1992). See also *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992).

15       Applicant asserts that since the process for mounting the driver chip and the applicable field of the driver chip disclosed in the cited reference are significantly different from the present invention, and the fact that the cited reference does not suggest or teach the conception of the chip thinning technology for solving the concerning problem of liquid crystal display module of the present invention, the cited 20 reference and the admitted prior art of the present invention cannot be combined in the manner suggested. Reconsideration of claims 1 and 13 is respectfully requested. As claims 3-6 and 14-19 are dependent upon claims 1 and 13, applicant asserts that if claims 1 and 13 are found allowable, claims 3-6 and 14-19 should additionally be found allowable.

25       Additionally, when making a rejection on prior art, the effective filing date of the cited reference shall be determined at first, so as to substantiate the prior art serving as a qualified cited reference. In conformity with MPEP 706.02 V(c), if a U.S. application claims foreign priority under 35 U.S.C. 119(a)-(d), the effective filing date 30 is the filing date of the U.S. application. Although the filing date of the foreign

priority document may be used to overcome certain references, the filing date of the foreign priority document is not the effective filing date.

Sato, one of the cited references relied upon by the Examiner, serves as the 5 foreign application whose priority benefit was claimed by the later filed U.S. counterpart application numbered 11/299,812, filed on December 13, 2005. In accordance with the above-referenced regulations set forth in MPEP 706.02 V(c), the filing date of the U.S. counterpart application number 11/299,812 is the effective filing date, which is posterior to the filing date of the present application submitted on 10 September 29, 2004. Therefore, the U.S. counterpart application 11/299,812 fails to serve as an effective cited reference relied upon for rejecting claims 1, 3-6 and 8-19 of the present invention.

15 **New Claims 20-21**

Dependent claims 20, 21 have been added as device claims to describe an embodiment of the present invention. Specifically, claims 20 and 21 are added to describe the state that either the gate driver chip or the source driver chip would be 20 bendable after its thickness is maintained below 0.3 mm. No new matter was used in the above claims.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,



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10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)